

Timing diagram for a 4-bit ripple-carry adder. The diagram shows the propagation of a carry signal from the least significant bit (CLK1) to the most significant bit (Out). The signals are labeled CLK1, D, A, B, C, CLK2, and Out. The Out signal is shown with a delay relative to the other signals, indicated by an arrow.

Fig. 1B

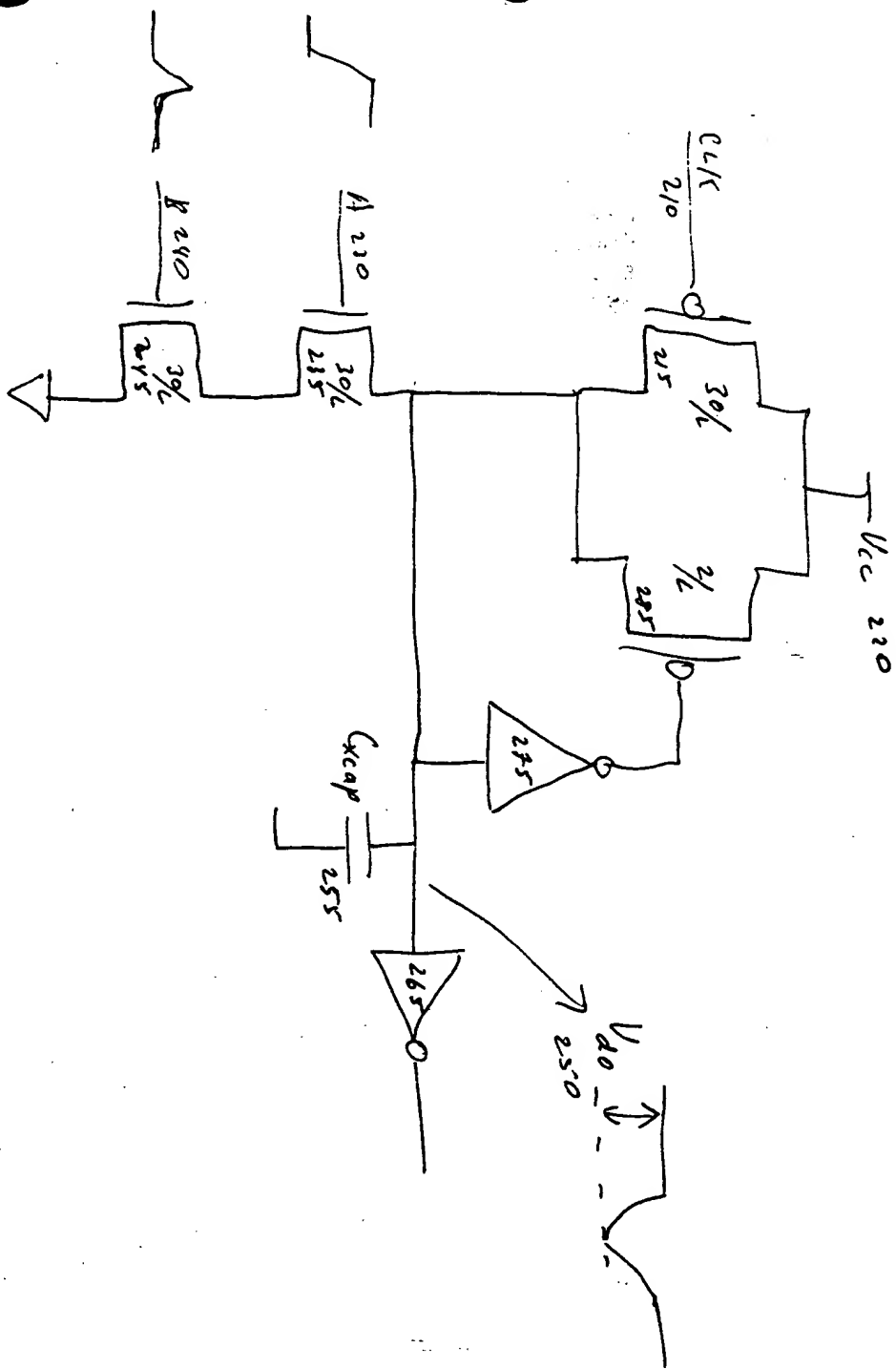


Fig. 2



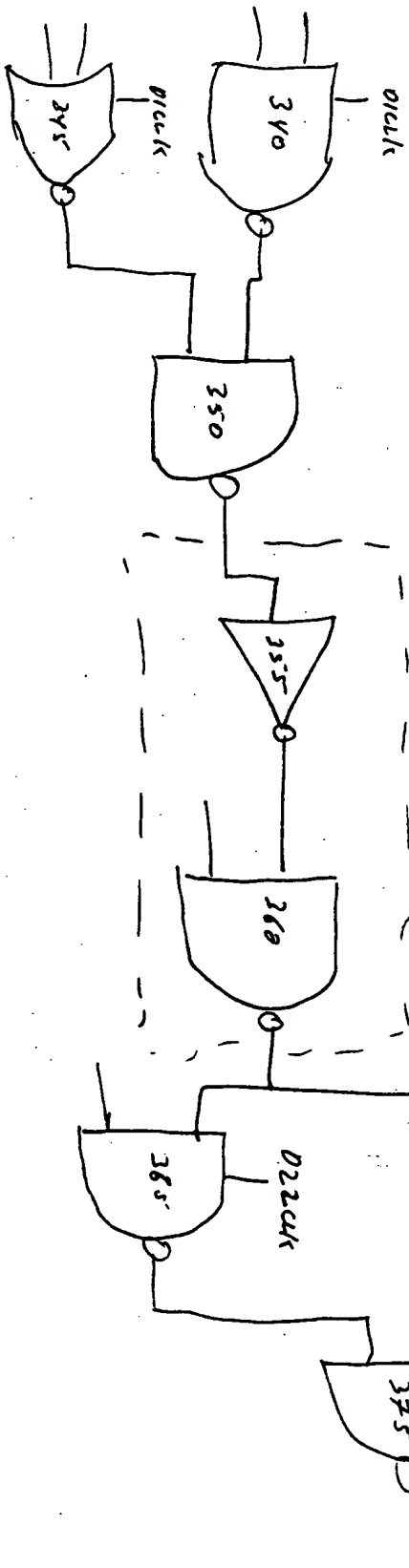
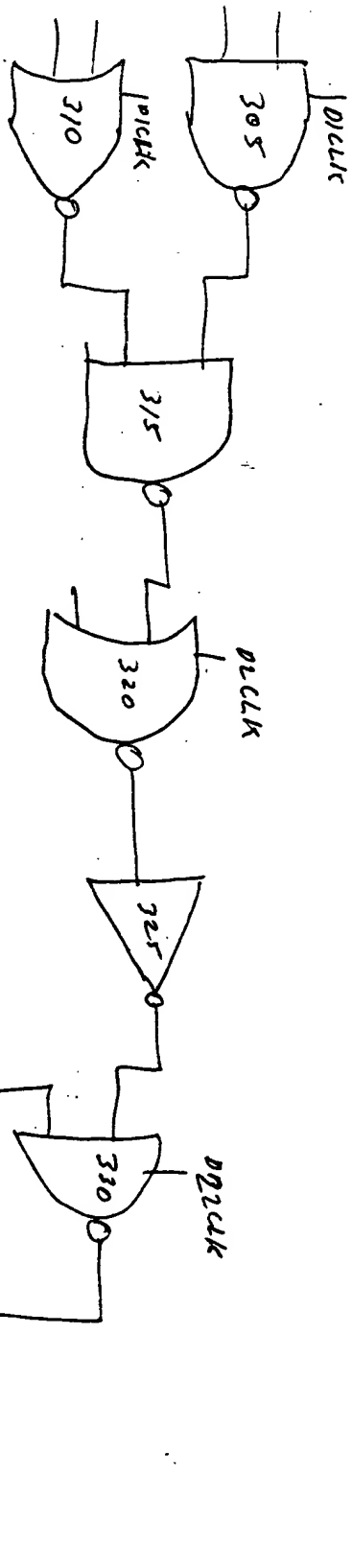


Fig. 3





SECRET 4750460

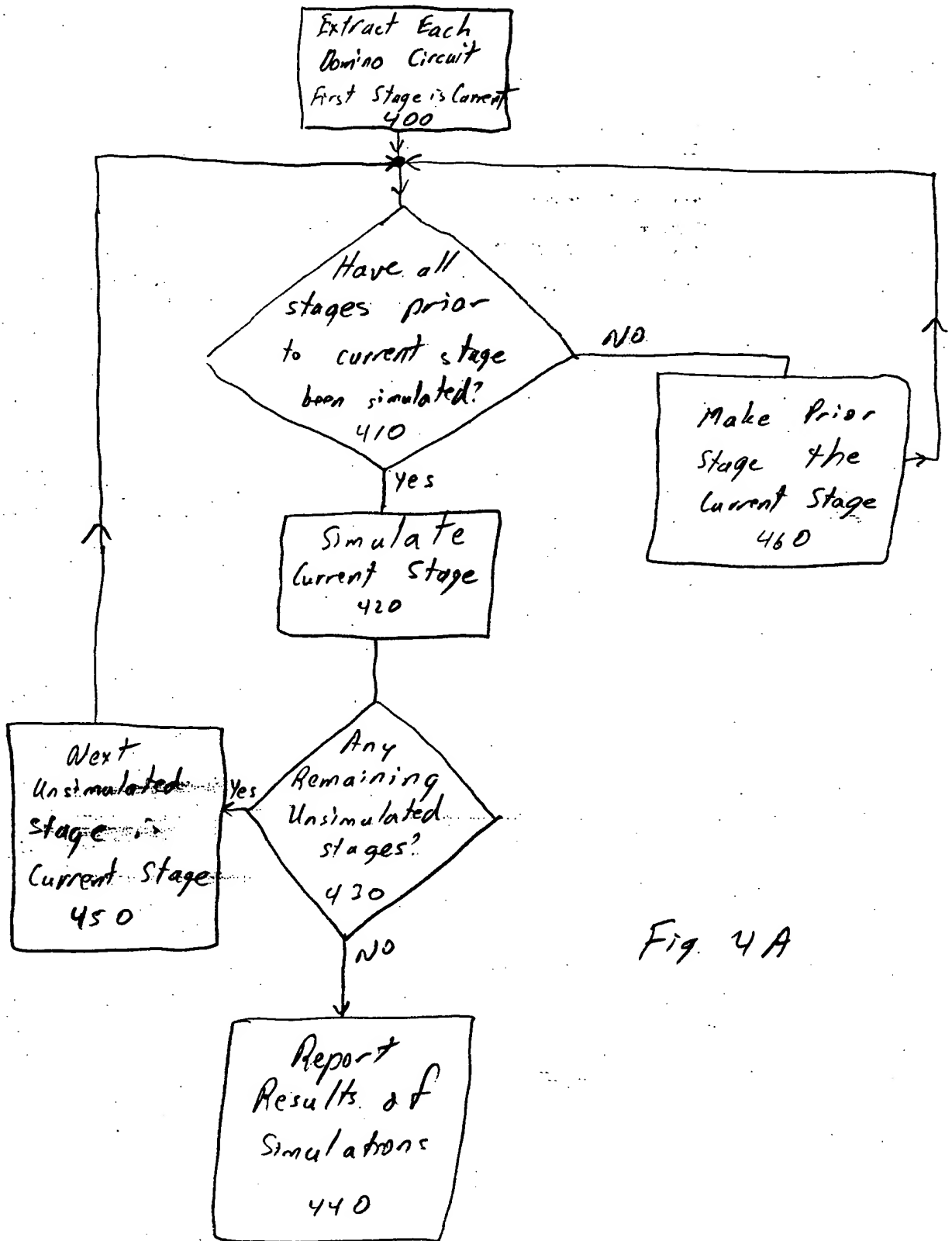


Fig 4A



SECRET

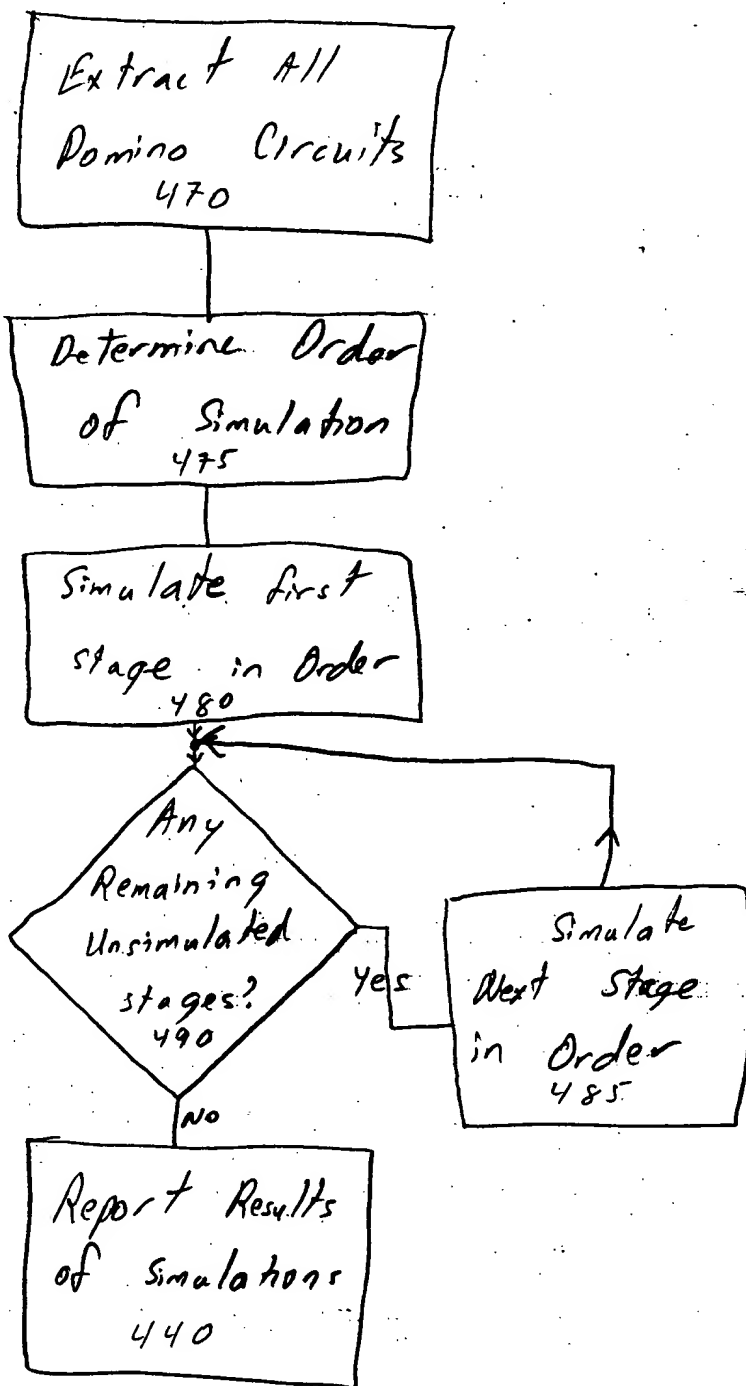


Fig. 4B



SECRET

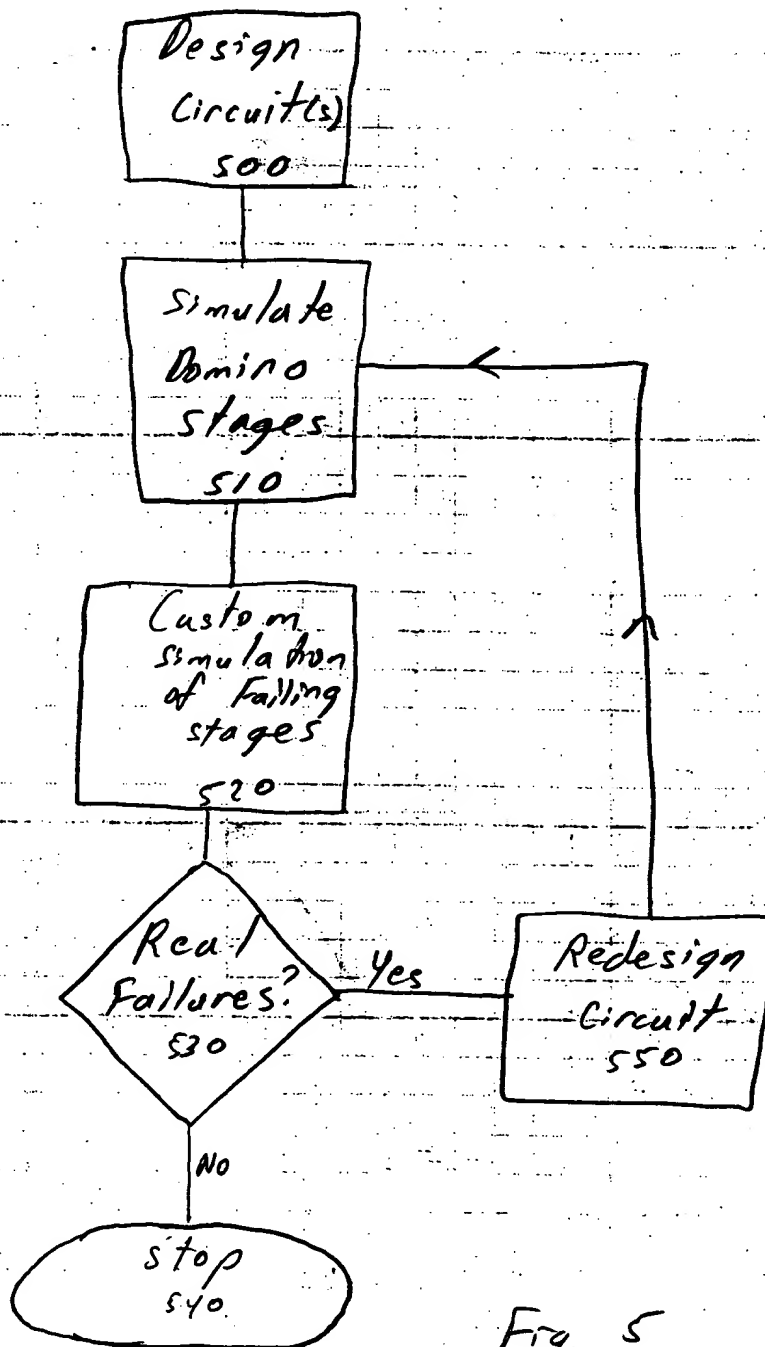


Fig. 5

Fig. 6

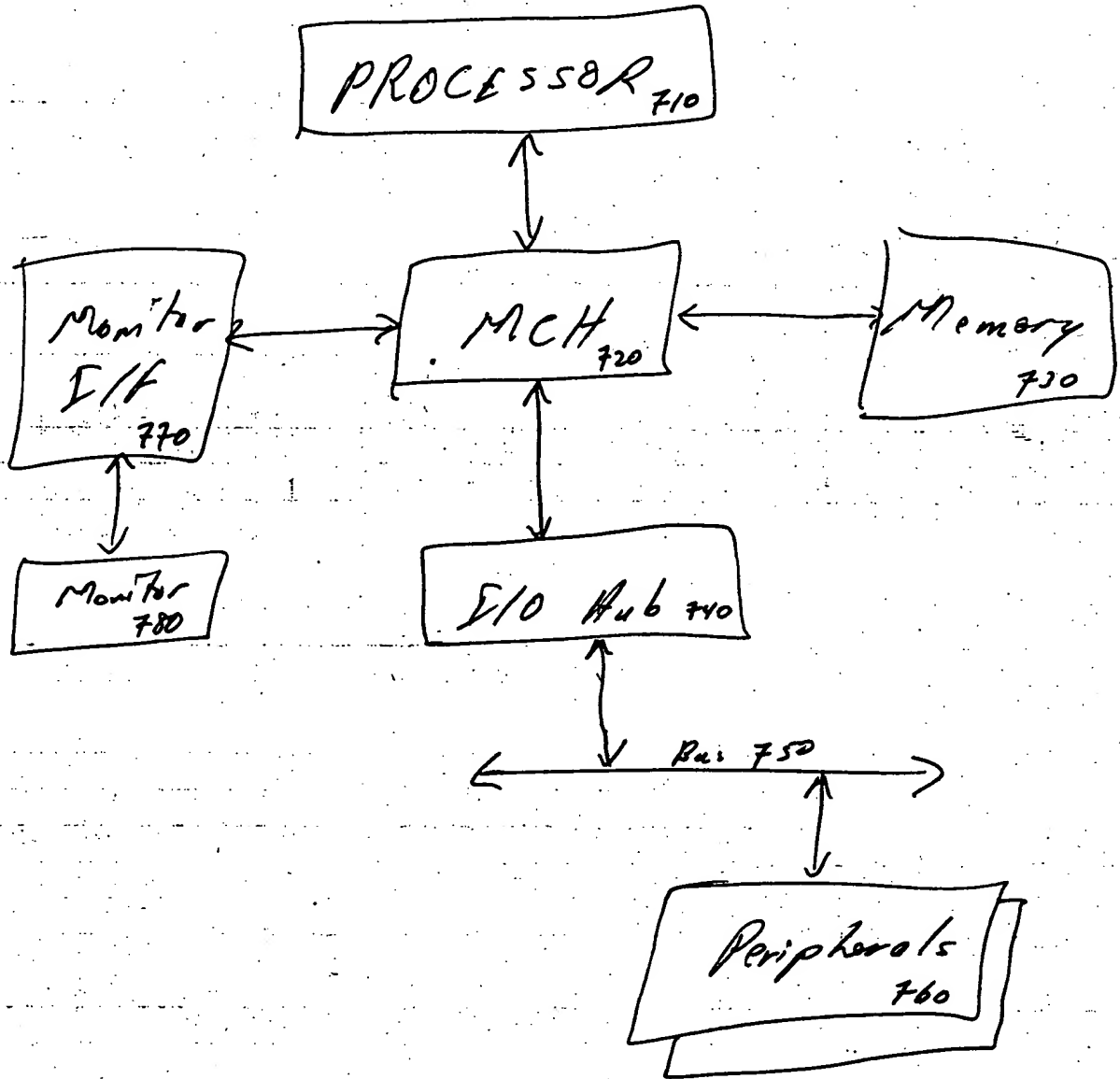


Fig. 7